What is claimed is:

1. A background memory manager (BMM) for managing a memory in a data processing system, the BMM comprising:

circuitry for transferring data to and from an outside device and to and from a memory;

a memory state map associated with the memory; and

a communication link to a processor;

characterized in that the BMM manages the memory, determining if each data structure fits into the memory, deciding exactly where to place the data structure in memory, performing all data transfers between the outside device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location.

2. The BMM of claim 1 wherein the BMM, in the process of storing each data structure, provides a data identifier for the structure on the link to the processor.

3. The BMM of claim 2 wherein the BMM, in making memory transactions, updates the memory state map to the new memory state, keeping track of regions occupied by valid data and regions not occupied by valid data.

4. The BMM of claim 2 wherein the BMM, in response to a signal on the processor link that the processor is finished with certain identified data in the memory, copies the data from the memory, if needed, to another device, and updates the memory state map to indicate the region of the data copied.

5. The BMM of claim 1 further comprising an interrupt handler allowing a remote data source to interrupt the BMM when data is available to be transferred to the memory.

6. The BMM of claim 1 wherein the data handled by the BMM constitutes network data packets.

7. A data processing system, comprising:

a processor;

a memory coupled to the processor; and

a background memory manager coupled to the memory and the processor, the background memory manager including circuitry for transferring data to and from an outside device and to and from the memory, and a memory state map associated with the memory;

characterized in that the BMM manages the memory, determining if each data structure fits into the memory, deciding exactly where to place the data structure in memory, performing all data transfers between the outside device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location.

8. The data processing system of claim 7 wherein the BMM, in the process of storing data structures in the memory, provides a data identifier for the structure to the processor.

9. The data processing system of claim 8 wherein the BMM, in making memory transactions, updates the memory state map to the new memory

state, keeping track of regions occupied by valid data and regions not occupied by valid data.

10. The data processing system of claim 8 wherein the BMM, in response to a signal from the processor that the processor is finished with certain identified data in the memory, copies the data, if necessary, from the memory to another device, and updates the memory state map to indicate the region of the data copied.

11. The data processing system of claim 7 further comprising an interrupt handler allowing a remote data source to interrupt the BMM when data is available to be transferred to the memory.

12. The data processing system of claim 7 wherein the data handled by the BMM constitutes network data packets.

13. A network packet router, comprising:

an input/output (I/O) device for receiving and sending packets on the network;

a processor;

a memory coupled to the processor; and

a background memory manager coupled to the memory and the processor, the background memory manager including circuitry for transferring packets to and from the I/O device and to and from the memory, and a memory state map associated with the memory;

characterized in that the BMM manages the memory, determining if each data structure fits into the memory, deciding exactly where to place the data structure in memory, performing all data transfers between the outside

device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location.

14. The data router of claim 13 wherein the BMM, in the process of storing a packet into the memory, provides a data identifier for the packet to the processor.

15. The data router of claim 14 wherein the BMM, in making memory transactions, updates the memory state map to the new memory state, keeping track of regions occupied by valid packets and regions not occupied by valid packets.

16. The data router of claim 14 wherein the BMM, in response to a signal that the processor is finished with a packet in the memory, copies the packet, if necessary, from the memory to the I/O device, and updates the memory state map to indicate the region of the packet copied.

17. The data router of claim 13 further comprising an interrupt handler allowing the I/O device to interrupt the BMM when packets are available to be transferred to the memory.

18. A method for managing a memory in a data processing system having a processor, comprising the steps of:

(a) transferring data structures to and from an outside device and to and from the memory by circuitry in a background memory manager (BMM);

(b) determining by the BMM if each data structure from the outside device will fit into available space in the memory;

(c) deciding by the BMM exactly where in the memory to store each data structure; and

(d) updating a memory state map associated with the memory in the BMM each time a memory transaction is made.

19. The method of claim 18 wherein, in step (c), the BMM, in the process of storing a data structure into the memory, provides a data identifier for the structure on the link to the processor.

20. The method of claim 19 wherein the BMM, in step (b), in making memory transactions, updates the memory state map to the new memory state, keeping track of regions occupied by valid data and regions not occupied by valid data.

21. The method of claim 19 wherein, in step (a), the BMM, in response to a signal that the processor is finished with certain identified data in the memory, copies the data, if necessary, from the memory to another device, and updates the memory state map to indicate the region of the data copied.

22. The method of claim 18 further comprising a step for interrupting the BMM by the outside device when data is available to be transferred to the memory.

23. The method of claim 18 wherein the data handled by the BMM constitutes network data packets.

24. The method of claim 23 wherein the network is the Internet.